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05SCS11/05SCE11

First Semester M.Tech. Degree Examination, May / June 08
Computer Architecture

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions***

1 a. List and explain the classification of Computer Architecture based on the notion of number of instruction streams and data streams that the processor handles. **(08 Marks)**

b. With a relevant block diagram, explain UMA and NUMA shared memory multiprocessor models. **(08 Marks)**

c. Consider the execution of an object code with 2,00,000 instructions on a 40 MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment :

Instruction type	CPI	Instruction mix
Arithmetic and logic	1	60 %
Load / store with cache hit	2	18 %
Branch	4	12 %
Memory reference with cache miss	8	10 %

i) Calculate the average CPI when the program is executed on a uniprocessor with the above trace results.

ii) Calculate the corresponding MIPS rate based on the CPI obtained. **(04 Marks)**

2 a. With suitable example, explain the different kinds of dependencies that may occur in 'straight – line code' between subsequent instructions. Also explain how the 'bypassing' helps in minimizing the pipeline stalls due to define – use and load – use conflicts. **(10 Marks)**

b. With suitable example and block diagram, representation distinguish CPA from CSA. Also, draw the block diagram of a pipeline unit for fixed – point multiplication of 8 – bit integers. **(10 Marks)**

3 a. Consider the following pipeline reservation table :

	0	1	2	3	4	5
S_1	X				X	
S_2			X			
S_3		X		X		X

i) List the Forbidden set and collision vector ii) Draw the state transition diagram iii) List the simple cycles and greedy cycles iv) Determine MAL v) Determine upper – bound and lower – bound on MAL vi) Determine the throughput of this pipeline if the clock frequency is 50 MHz. **(12 Marks)**

b. Explain the implementation of super scalar CISC using super scalar RISC core. **(08 Marks)**

4 a. With neat diagram, explain the principle of operation of ROB. What is the role of ROB in 'speculative execution'? **(10 Marks)**

b. Discuss any three factors that affect the performance of an interconnection network. **(06 Marks)**

c. Consider the execution of a program of 15,000 instructions by a five stage linear instruction pipeline with a clock rate of 25MHz. The penalties due to branch instructions and out – of – sequence executions are ignored.
i) Calculate the speed up factor in using this pipeline to execute the program as compared with the use of equivalent nonpipelined processor with an equal amount of flow through delay. ii) Find the efficiency and throughput of this pipelined processor. iii) Draw a Reservation table for this pipeline. **(04 Marks)**

5 a. List the important characteristics of fine – grained SIMD architecture. **(04 Marks)**
b. With a neat block diagram, explain the processing element structure and connectivity structure of CM5. **(10 Marks)**
c. What is Vectorization? Explain how the computation can be speeded up with vectorization. **(06 Marks)**

6 a. Discuss the cache coherence problems in data sharing and in process migration with respect to multiprocessor system. **(10 Marks)**
b. Explain the concept of Directory based cache coherence scheme. **(10 Marks)**

7 a. Explain the characteristics features of Data Flow Computers. Compare static versus dynamic Data Flow Computers. **(10 Marks)**
b. Draw the Data Flow Graph for the calculation of cos(x) using the series :

$$\text{Cos}(x) = 1 - \frac{x^2}{2!} + \frac{x^4}{4!} - \frac{x^6}{6!} \cdot$$ **(04 Marks)**

c. Discuss any one method of connection, which can implement all communication patterns based on program demands. **(06 Marks)**

8 a. Explain the principle of VLIW processor and compare it with superscalar processors. **(10 Marks)**
b. Write short notes on:
i) SPARC architecture
ii) Power PC 620. **(10 Marks)**

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